



Interactions Between Indirect DC-Voltage Estimation and Circulating Current Controllers of MMC-Based HVDC Transmission Systems

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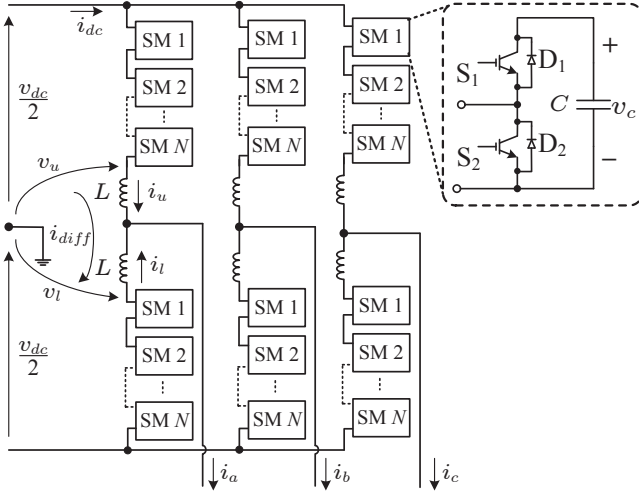


Fig. 2. Three-phase MMC circuit topology.

while existing methods use only SM capacitor voltages/energy. Owing to the use of switching signals, the proposed technique is able to operate independently from the circulating current controller. Results demonstrate that the proposed strategy is able to deliver steady-state and transient performance similar to the direct dc-voltage control regardless of the two different circulating current control methods. Moreover, the adopted PR circulating current controller [12] demonstrates better SM capacitor voltage regulation compared to the DFSRF-based circulating current controller.

The structure of the paper is as follows. Section II describes the MMC topology and circulating current control techniques. Section III analyses the proposed dc-voltage estimation method and alternative methods. A detailed analysis on SM capacitor voltages and the impact on dc-voltage estimations are presented in Section IV. Section V provides the simulation results based on a real-time digital simulator (RTDS) and the conclusions are summarized in Section VI.

II. MMC OPERATION AND CONTROL

A. MMC Topology

The MMC circuit topology (Fig. 2) has been well described in the existing literature [2], [3]. One MMC phase-leg consists of two arms which include N series-connected SMs, and one inductor (L) per arm. The SM capacitor voltages in the upper and lower arms are defined as v_{Cuj} and v_{Clj} for $j = \{1, 2, \dots, N\}$, respectively. Various modulation techniques can be applied [25], and capacitor voltage balancing can be achieved by adopting a sort-and-select algorithm [17], which defines the state (insert or bypass) of the SMs. s_{uj} and s_{lj} are the switching signals of upper and lower arms, and v_{dc} is the instantaneous dc-voltage. Assuming identical semiconductor devices, and that the switch and the anti-parallel diode of each device have equal forward voltage (V_f) and equal on-resistance (R_{on}), the voltages applied to the extremes of the upper and lower arm inductors (v_u and v_l) are:

$$v_u = \frac{v_{dc}}{2} - \sum_{j=1}^N \left(s_{uj} \cdot v_{Cuj} + i_u R_{on} + \text{sgn}(i_u) \cdot V_f \right), \quad (1)$$

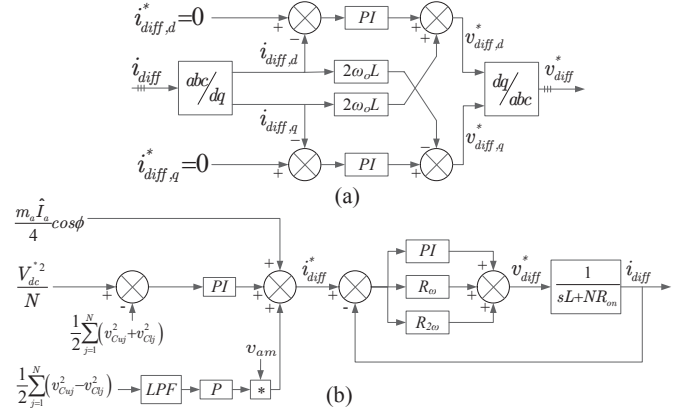


Fig. 3. Circulating current controller: (a) CCSC [14] and (b) FCCC [12].

$$v_l = -\frac{v_{dc}}{2} + \sum_{j=1}^N \left(s_{lj} \cdot v_{Clj} - i_l R_{on} - \text{sgn}(i_l) \cdot V_f \right). \quad (2)$$

The common and differential mode currents (i_{comm} and i_{diff}) can be expressed in terms of upper arm current (i_u), lower arm current (i_l), and output current (i_a) as $i_{comm} = (i_u + i_l)/2 = i_a/2$ and $i_{diff} = (i_u - i_l)/2$, respectively [12]. The differential current is also referred to as circulating current. Subsequently, the common and differential mode voltages (v_{comm} and v_{diff}) can be defined using v_u and v_l as $v_{comm} = (v_u + v_l)/2$ and $v_{diff} = (v_u - v_l)/2$, respectively [12].

B. Circulating Current Control Techniques

Second order harmonic suppression, SM capacitor voltage regulation, and upper/lower arm energy balancing can be achieved by means of circulating current control within a phase-leg. Two prevalent circulating current control techniques [12] and [14] are adopted in this study to represent the main two categories mentioned in Fig. 1.

1) *Circulating Current Suppression Control (CCSC)*: The differential current in a phase-leg can be modeled as a second harmonic circulating component superimposed on one-third of the total dc current ($I_{dc}/3$) [14]. Thus, the three-phase circulating currents can be transformed to two dc components ($i_{diff,d}$ and $i_{diff,q}$) in the DFSRF. The steady-state second harmonic circulating current is of negative sequence. CCSC configuration is shown in Fig. 3(a). The dc components $i_{diff,d}$ and $i_{diff,q}$ are driven to zero using PI controllers in order to suppress the second harmonic circulating current. The dc circulating current control, average SM energy regulation, and upper/lower arm energy balancing are not included in CCSC technique.

2) *Forced Circulating Current Control (FCCC)*: The three inputs of Fig. 3(b) define the overall differential current reference (i_{diff}^*). The first input defines the dc component of i_{diff}^* in order to maintain the power balance within the phase-leg. The second input determines an additional dc current component which maintains the average energy in the SM capacitors. The action of the PI controller drives SM energy to its reference in steady-state. The third input adds a fundamental-frequency component to balance the energy between upper and

lower arms. The sum of three reference inputs is fed into a current controller (Fig. 3(b)) which consists of a PI controller, and a set of resonant controllers tuned at fundamental and second-harmonic frequency (R_ω , $R_{2\omega}$). Detailed description of FCCC can be found in [12].

III. DC-VOLTAGE ESTIMATION AND CONTROL

Measurement-based direct dc-voltage control is the simplest approach but requires high-voltage sensors. Thus, estimation-based indirect dc-voltage control is a likely alternative for MMC-HVDC. Indirect dc-voltage control of MMC-based BTB systems are reported in [22], [23]. The arithmetical average voltage of all the SM capacitors [22], and the MMC average energy [23], are regulated in the high-level controllers, in order to indirectly control the dc-voltage.

When the estimation methods of [22] and [23] are applied to control the dc-voltage of MMC-HVDC, the SM capacitor voltages are directly controlled by the high-level controller. Thus, the existing dc-voltage estimations strongly depend on the instantaneous SM capacitor voltages, and the indirect dc-voltage control interacts with the circulating current controller. The proposed method controls only the output voltages of the SMs owing to the use of MMC switching function. Hence, the proposed dc-voltage estimation is not affected by the instantaneous SM capacitor voltage behavior and mutual interactions can be avoided between indirect dc-voltage control and circulating current control (i.e. SM capacitor voltage regulation (Fig. 3)).

Regardless of the dc-voltage realization method (measurement or estimation), the well-established decoupled current control [14] can be used to regulate the dc-voltage. Fig. 4 shows the overall control structure with high-level indirect dc-voltage control. Analysis on the proposed instantaneous dc-voltage estimation method and alternative methods are illustrated here.

A. Proposed DC-Voltage Estimation Method (EM-1)

The proposed instantaneous dc-voltage estimation method is based on Kirchhoff's voltage law (KVL). At any given time instant, the voltage across the dc-link of one MMC phase-leg is equal to the sum of upper arm switched-voltage, lower arm switched-voltage, voltage across two arm inductors, and the voltage drop in all conducting semiconductor devices. Using (1) and (2), the instantaneous dc-voltage of a phase-leg is:

$$v_{dc} = \sum_{j=1}^N \left\{ s_{uj} \cdot v_{Cuj} + s_{lj} \cdot v_{Clj} + 2R_{on} \cdot i_{diff} + V_f \cdot [\text{sgn}(i_u) - \text{sgn}(i_l)] \right\} + 2L \frac{di_{diff}}{dt}. \quad (3)$$

Considering the three phases ($x = a, b, c$) and assuming $V_f \ll v_C$, the instantaneous dc-voltage of the MMC can be estimated as:

$$v_{dc(EM-1)} = \frac{1}{3} \sum_{x=a,b,c} \sum_{j=1}^N \{ s_{ujx} \cdot v_{Cujx} + s_{ljx} \cdot v_{Cljx} \} + \frac{2}{3} NR_{on} i_{dc} + \frac{2}{3} L \frac{di_{dc}}{dt}. \quad (4)$$

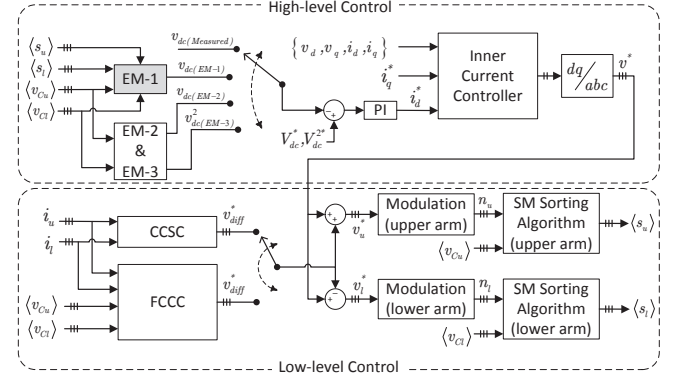


Fig. 4. Overall control structure of the dc-voltage controlling MMC

It is noteworthy that similar theoretical definitions for the MMC dc-voltage based on KVL can be found in the literature, considering ideal semiconductor devices [21], [26]. However, application of those definitions in estimation-based indirect dc-voltage control of MMC-HVDC and its performance combined with different circulating current control techniques have not been investigated yet. The proposed dc-voltage estimation (EM-1), accounts for the voltage drops in semiconductor devices. Moreover, the proposed method estimates the dc-voltage using the MMC switching function in addition to SM capacitor voltages while the existing estimation methods use only SM capacitor voltages.

Use of the SM switching function generates noise in the estimated dc-voltage ($v_{dc(EM-1)}$). A standard unity gain ($k = 1$) second order low pass filter (5) can be used [27].

$$H(s) = \frac{k\omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2}. \quad (5)$$

The damping ratio (ξ) is chosen to be unity, in order to provide a critically damped filter response [27]. The cut-off frequency (ω_c) can be specified to be less than the switching frequency while a minimum ω_c should be chosen as $\omega \leq 0.1\omega_c$ so dynamics of the dc-voltage during transients are not affected [27].

The estimated dc-voltage of (4) is regulated to the reference (V_{dc}^*). As the dc-voltage is estimated using the SM switching function, the high-level controller controls only the capacitor voltages of the activated SMs (i.e. output voltage of the SMs). Hence, the SM capacitor voltage regulation, which is an objective of low-level control, does not directly interact with the high-level indirect dc-voltage control.

B. Overall SM Capacitor Voltage Control (EM-2)

Standard modulation methods [3] do not deviate the average number of inserted SMs from N over a fundamental period, while certain modulation methods such as those of [28], [29] substantially change the average number of inserted SMs. Considering a standard modulation method, the arithmetic average of SM capacitor voltages (v_C) is:

$$v_C = \frac{1}{6N} \sum_{x=a,b,c} \sum_{j=1}^N (v_{Cujx} + v_{Cljx}). \quad (6)$$

Most of the harmonics, with the exception of triplen ones, cancel among the phases. Thus, v_C does not contain fundamental or second order harmonics [22], and represents a dc-voltage assuming triplen harmonics are not present.

The method of [22] is adapted to the MMC-HVDC system, including the voltage drops in semiconductor devices as:

$$v_{dc(EM-2)} = \frac{1}{3} \sum_{x=a,b,c} N v_C + \frac{2}{3} N R_{on} i_{dc} + \frac{2}{3} L \frac{di_{dc}}{dt} \quad (7)$$

The calculated voltage v_C (6) is regulated to the reference V_C^* (8), in order to indirectly regulate the dc-voltage to its reference V_{dc}^* , as follows:

$$V_C^* = \frac{V_{dc}^*}{N} - \frac{2}{3} R_{on} i_{dc} - \frac{2}{3N} L \frac{di_{dc}}{dt}. \quad (8)$$

Combining (7) and (8), the dc-voltage can indirectly be controlled by regulating v_C :

$$(V_C^* - v_C) = \frac{1}{N} (V_{dc}^* - v_{dc(EM-2)}). \quad (9)$$

A PI controller can be used to drive the steady-state error of v_C to zero (Fig. 4).

C. MMC Total Energy Control (EM-3)

DC-voltage can be indirectly controlled by means of the stored energy in MMC SMs either by regulating single SM energy, or the total energy (factor of $1/6N$) [23]. The average of squared capacitor voltages (e_C) is proportional to, and can be used to represent the average energy of SMs as:

$$e_C = \frac{1}{6N} \sum_{x=a,b,c} \sum_{j=1}^N (v_{C_{ujx}}^2 + v_{C_{ljx}}^2). \quad (10)$$

In the implementation of [23], the impact of arm inductors and R_{on} of semiconductors is considered to be negligible. Since e_C is approximately equal to v_C^2 , and based on the assumptions, (7) can be modified with (10) as:

$$v_{dc(EM-3)}^2 = N^2 e_C, \quad (11)$$

which estimates the dc-voltage in terms of the stored energy. e_C is regulated to the reference $E_C^* = V_{dc}^{*2}/N^2$, in order to indirectly control the dc-voltage, based on the error of:

$$(E_C^* - e_C) = \frac{1}{N^2} (V_{dc}^{*2} - v_{dc(EM-3)}^2). \quad (12)$$

IV. IMPACT OF SM CAPACITOR VOLTAGES AND CIRCULATING CURRENT CONTROL ON DC-VOLTAGE ESTIMATIONS

DC-voltage estimation and indirect control methods are based on SM capacitor voltages which are closely related to the power fluctuation in MMC arms. Therefore, SM capacitor voltage function should be quantified in order to demonstrate its effects on the proposed and existing dc-voltage estimations.

A. Submodule Capacitor Voltage Function

One MMC phase-leg (phase a) is considered for the derivations. Similar equations are valid for other two phase-legs ($x = b, c$) with appropriate phase shifts. When a capacitor voltage balancing algorithm is applied and if the SM switching frequency is relatively high, the following two assumptions can be made for steady-state balanced operation.

1) N SM capacitor voltages within each arm (upper/lower) are equal and denoted by v_{Cu} and v_{Cl} .

$$v_{Cu} = \bar{V}_C + \Delta v_{Cu} \quad v_{Cl} = \bar{V}_C + \Delta v_{Cl} \quad (13)$$

The dc component/average value (\bar{V}_C) of v_{Cu} and v_{Cl} is assumed to be equal amongst three phases, based on the balanced operation of MMC. Only the ac/ripple components of v_{Cu} and v_{Cl} (denoted as Δv_{Cu} , Δv_{Cl}) are different.

2) The duty ratio of each arm (upper/lower) is evenly distributed among the SMs and denoted by d_u and d_l [12]:

$$d_u = (1 - v_{am} - v_{2am})/2 \quad d_l = (1 + v_{am} - v_{2am})/2, \quad (14)$$

where $v_{am} = m_a \cos(\omega t)$ represents the normalized output voltage reference, and the modulation index (m_a) is within the range $[0, 1]$. $v_{2am} = m_{2a} \sin(2\omega t + \phi_2)$ is the reference waveform of the injected second order harmonic voltage in order to suppress/eliminate the second harmonic circulating current, or to inject a desired second harmonic circulating current which reduces the capacitor voltage ripple [12]. m_{2a} is the modulation index of the injected second harmonic voltage.

The output current (i_a) and differential current (i_{diff}) can be defined as $i_a = \hat{I}_a \cos(\omega t + \phi)$ and $i_{diff} = I_{dc}/3 + \hat{I}_{2a} \cos(2\omega t + \phi_2)$. The second harmonic component of i_{diff} can be either a residual circulating current or an injected desired circulating current. The upper and lower arm currents can be defined as:

$$i_u = \frac{I_{dc}}{3} + \frac{\hat{I}_a}{2} \cos(\omega t + \phi) + \hat{I}_{2a} \cos(2\omega t + \phi_2), \quad (15)$$

$$i_l = -\frac{I_{dc}}{3} + \frac{\hat{I}_a}{2} \cos(\omega t + \phi) - \hat{I}_{2a} \cos(2\omega t + \phi_2). \quad (16)$$

The output power of one upper/lower SM can be expressed as $p_{SMu} = i_u \cdot (d_u v_{Cu})$ and $p_{SMl} = -i_l \cdot (d_l v_{Cl})$. In steady-state, no dc-power component appears in p_{SMu} and p_{SMl} [12]. The SM power can also be given in terms of the SM capacitor voltage as:

$$p_{SMu} = \frac{1}{2} C \frac{dv_{Cu}^2}{dt} \quad p_{SMl} = \frac{1}{2} C \frac{dv_{Cl}^2}{dt}, \quad (17)$$

where C is the SM capacitance. Solving (17) with the definition in (13), gives:

$$\Delta v_{Cu} = \frac{1}{C} \int \frac{p_{SMu}}{v_{Cu}} dt \quad \Delta v_{Cl} = \frac{1}{C} \int \frac{p_{SMl}}{v_{Cl}} dt. \quad (18)$$

Substituting SM power in (18), solutions can be obtained for Δv_{Cu} and Δv_{Cl} . Based on $m_{2a} \ll m_a$ and $\hat{I}_{2a} \ll \hat{I}_a$, terms with small magnitudes are neglected in the solutions. Hence, the simplified expressions for v_{Cu} and v_{Cl} are:

$$v_{Cu} = \bar{V}_C + \frac{\hat{I}_a}{4\omega C} \sin(\omega t + \phi) - \frac{m_a I_{dc}}{6\omega C} \sin(\omega t) - \frac{m_a \hat{I}_a}{16\omega C} \sin(2\omega t + \phi), \quad (19)$$

$$v_{Cl} = \bar{V}_C - \frac{\hat{I}_a}{4\omega C} \sin(\omega t + \phi) + \frac{m_a I_{dc}}{6\omega C} \sin(\omega t) - \frac{m_a \hat{I}_a}{16\omega C} \sin(2\omega t + \phi). \quad (20)$$

In order to find \bar{V}_C , (21) can be obtained by applying KVL to the MMC phase-leg,

$$v_{dc} = N(d_u v_{Cu} + d_l v_{Cl}) + 2N R_{on} i_{diff} + 2L \frac{di_{diff}}{dt}. \quad (21)$$

In steady-state balanced operation, m_a , \hat{I}_a , and v_{dc} are common amongst the three phases. Substituting (14), (19), (20) in (21), and considering the equivalent equations for three phases, \bar{V}_C can be expressed as:

$$\bar{V}_C = \frac{v_{dc}}{N} + \frac{m_a \hat{I}_a}{8\omega C} \sin(\phi) - \frac{m_a m_{2a} \hat{I}_a}{32\omega C} \cos(\phi - \phi_2) - \frac{2}{3} R_{on} i_{dc} - \frac{2}{3N} L \frac{di_{dc}}{dt}. \quad (22)$$

The ac components in (22) cancel between the three phases, and the dc term with a large denominator ($32\omega C$) and a small numerator ($m_a m_{2a}$) is insignificant as ($0 \leq m_{2a} \ll m_a \leq 1$).

It can be concluded that \bar{V}_C specifically depends on reactive power, as \bar{V}_C in (22) contains an additional dc component with $\sin(\phi)$ apart from the semiconductor voltage drops and arm inductor voltage drops. Thus, SM capacitor voltages can be higher or lower than the rated value depending on reactive power sign and the reference at the PCC.

B. Impact of SM Capacitor Voltages

This section analyses the effect of SM capacitor voltages on dc-voltage estimations, assuming SM capacitor voltages are balanced and identical within each arm, where the balancing algorithm is applied.

1) *Impact on EM-1:* Assuming that the duty ratio of each arm is evenly distributed among the SMs ($d_{ix} = \frac{1}{N} \sum_{j=1}^N s_{ijx}$; ($i = u, l$)), $v_{dc(EM-1)}$ can be calculated by substituting (19), (20) in (4) and simplifying the results:

$$v_{dc(EM-1)} = N \left(\bar{V}_C - \frac{m_a \hat{I}_a}{8\omega C} \sin(\phi) + \frac{2}{3} R_{on} i_{dc} + \frac{2}{3N} L \frac{di_{dc}}{dt} \right). \quad (23)$$

Hence, substituting (22) in (23), $v_{dc(EM-1)} = v_{dc}$ shows that EM-1 estimates the dc-voltage with no error.

2) *Impact on EM-2:* According to Section III-B, v_C represents a dc component which should be the average voltage of SM capacitors (\bar{V}_C). Replacing v_C in (7) with \bar{V}_C in (22), shows that EM-2 estimates the dc-voltage with an error:

$$v_{dc(EM-2)} = v_{dc} + \frac{m_a N \hat{I}_a}{8\omega C} \sin(\phi). \quad (24)$$

For a given MMC configuration, the N/C ratio is constant (constant unit capacitance H_C [22]), so the estimation error depends on reactive power ($\sin \phi$), m_a , and \hat{I}_a .

3) *Impact on EM-3:* Substituting (19), (20), (22) in (10) and neglecting the terms with m_a^2 ($0 \leq m_a \leq 1$) and the terms with a large denominator ($\omega^2 C^2$), the arithmetic average of squared SM capacitor voltages is:

$$e_C = \frac{v_{dc}^2}{N^2} + \frac{m_a v_{dc} \hat{I}_a}{4N\omega C} \sin(\phi). \quad (25)$$

Semiconductor voltage drops in (22) are not considered in the substitution according to the assumptions of Section III-C. e_C represents a dc value as the ac components cancel between the three phases.

Hence, from (25) and (11), the effect of SM capacitor voltages on EM-3 is:

$$v_{dc(EM-3)}^2 = v_{dc}^2 + \frac{m_a N v_{dc} \hat{I}_a}{4\omega C} \sin(\phi). \quad (26)$$

Similarly to EM-2, the estimation error depends on reactive power ($\sin \phi$), m_a , \hat{I}_a , and v_{dc} .

C. Impact of Circulating Current Control

SM capacitor voltage analysis shows that the average SM capacitor voltage depends on reactive power, in addition to the voltage drops in semiconductor devices and arm inductors. Although N SMs are inserted on average within a phase-leg, the average voltage of SM capacitors is not naturally maintained at the $N : 1$ proportion of the total average voltage reflected across the N number of inserted SMs (i.e. V_{dc}/N in an ideal MMC). This phenomenon is not affected by the second harmonic component of the circulating current as shown in (22). However, an additional dc circulating current component can compensate for the offset of average SM capacitor voltages caused by the voltage drops in semiconductor devices, arm inductors, and the reactive power dependent dc component shown in (22).

CCSC only suppresses/eliminates the second harmonic circulating current (Fig. 3(a)). The dc component of the circulating current is necessary and it is naturally defined to maintain the power balance within phase-leg. Hence, the average SM capacitor voltage / energy is not regulated, and the reactive power dependent estimation errors of EM-2 and EM-3 cannot be compensated by CCSC.

FCCC defines the dc circulating current reference in order to maintain the power balance within the phase-leg, and to regulate the SM capacitor energy within the leg to its reference (Fig. 3(b)). The additional dc component which regulates the SM capacitor energy, compensates for the overall error in average SM capacitor voltage given by (22). Therefore, the estimation errors caused by semiconductor voltage drops, arm inductor voltage drops, and reactive power are compensated in all EM-1, EM-2, and EM-3, when FCCC is used.

V. SIMULATION RESULTS

A. CIGRE Benchmark MMC-HVDC Test System in RTDS

In order to demonstrate the performance of the estimation methods of Section III, a simulation model, derived from the CIGRE benchmark MMC-HVDC test system, is used. Fig. 5 shows a single-line diagram of the MMC-HVDC test system.

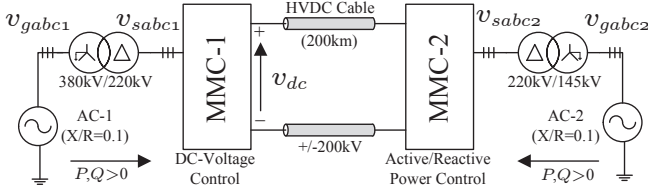


Fig. 5. Benchmark MMC-HVDC test system.

TABLE I
MMC-HVDC SIMULATION PARAMETERS

Rated Power	400 MVA
Number of SMs/arm (N)	16
DC-Voltage (V_{dc})	400 (± 200) kV
SM Capacitance (C)	800 μ F
SM Capacitor Voltage (V_C)	25 kV
SM ON-Resistance (R_{on})	0.00014 pu (17.013 m Ω)
Arm Inductance (L)	0.075 pu (29 mH)
Transformer Leakage Inductance	0.091 pu (35 mH)
Transformer Resistance	0.003 pu (0.363 Ω)
Carrier frequency (f_c)	2 kHz
System frequency (f)	50 Hz

A switching model of the benchmark MMC-HVDC system with 17-level MMCs (16 SMs per arm) is developed in an RTDS. The number of SMs per arm (N) for the switching model is selected based on the processing limitations of the real-time simulator and the SM capacitance is calculated by setting the stored energy per SM to 30 kJ/MVA [30]. Hence, the 17-level MMC-HVDC system represents the original benchmark system with 201-levels (200 SMs per arm) [22], [30]. Table I provides the parameters of MMC-HVDC system. Phase-disposition PWM and the active capacitor voltage balancing algorithm of [17] are adopted. Both CCSC and FCCC are used in MMC-1, which is the converter regulating the dc-link voltage. The direct voltage measurement as well as EM-1, EM-2, and EM-3 are used in MMC-1. MMC-2 is controlled with CCSC and operates in active/reactive power control mode.

B. Steady-State Operation

In steady-state, V_{dc}^* is set to 400 kV in MMC-1 and the AC-2 is set at 400 MW and 0 MVar. The derived capacitor voltage function of (19), (20), and (22) is verified with the instantaneous average of the simulated SM capacitor voltages in Fig. 6.

1) *Comparison of DC-Voltage Estimations*: The dc-voltage estimations of (4), (7), and (11) are calculated in steady-state under direct dc-voltage control. Fig. 7 shows the normalized estimations and measured dc-voltage with CCSC and FCCC. Fig. 7(a) demonstrates that EM-1 is more accurate compared to EM-2 and EM-3 with CCSC, and the errors observed in EM-2 and EM-3 agree well with (24) and (26), respectively. Moreover, Fig. 7(b) shows that EM-1 is unaffected by FCCC,

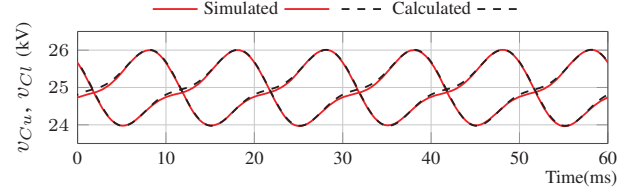


Fig. 6. Simulated and calculated SM capacitor voltages of phase a.

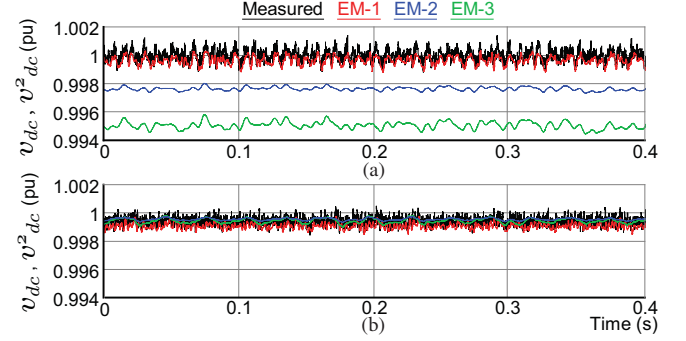


Fig. 7. Comparison of dc-voltage estimations EM-1,2,3: (a) with CCSC and (b) with FCCC.

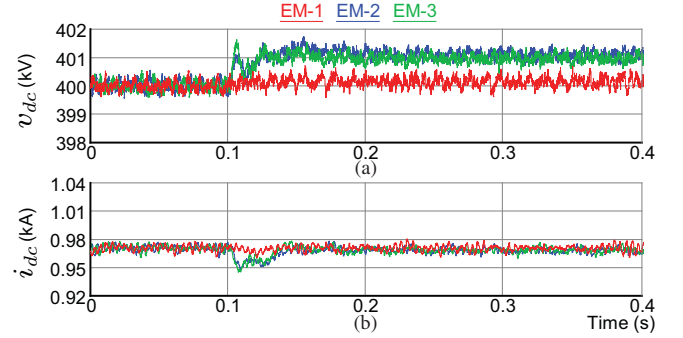


Fig. 8. DC-voltage control method changes from direct to indirect with CCSC: (a) dc-voltage and (b) dc current.

where the estimation errors of EM-2 and EM-3 become zero, proving the superior performance of FCCC in SM capacitor energy regulation. Thus, EM-1 provides a better estimation of the dc-voltage, irrespective of the circulating current controller. EM-2 and EM-3 have improved accuracy only with FCCC, due to the action of capacitor voltage regulation loop (Fig. 3(b)).

2) *Transition from Direct to Indirect DC-Voltage Control*: Initially, the circulating current controller is set by CCSC/FCCC, and MMC-1 is set to direct dc-voltage control. At $t = 0.1$ s, the dc-voltage control is switched from direct to indirect (EM-1, EM-2, and EM-3). Fig. 8 shows the response of dc-voltage and current with CCSC. The proposed EM-1 controls the dc-voltage as in direct dc-voltage control. When switched to EM-2 and EM-3, an offset is present in the dc-voltage as a result of the estimation errors. The dc current is significantly affected only in EM-2 and EM-3 during the transition.

Figs. 9(a) and 9(b) provide the response of the dc-voltage and current for EM-1 and EM-3 with FCCC. Both methods have similar performance except the dc-voltage has a slight

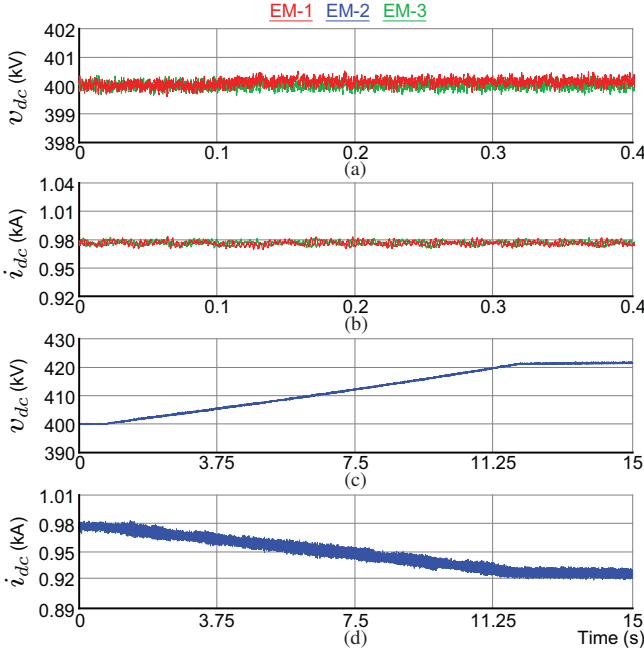


Fig. 9. DC-voltage control method changes from direct to indirect with FCCC: (a) dc-voltage (EM-1,3), (b) dc current (EM-1,3), (c) dc-voltage (EM-2) and (d) dc current (EM-2).

offset in EM-1. The small offset is a result of semiconductor voltage drops included in (4) which are already compensated by FCCC. Accordingly, Figs. 9(c) and (d) provide the dc-side response for EM-2 with FCCC. EM-2 has a stable steady-state with considerable offsets in both dc-voltage and current, following a long transient caused by the mutual interaction of the dc-voltage controller and the SM capacitor energy regulation loop of FCCC. Although the steady-state dc-voltage is stable for EM-2 with FCCC, accurate dc-voltage control cannot be achieved. Given that EM-2 does not have satisfactory performance in steady-state, and also it does not deliver adequate transient performance as perceived in simulations, EM-2 with FCCC is not considered in the transient performance results for the rest of the paper.

C. Active and Reactive Power Control

Initially, the MMC-HVDC system operates in steady-state. Based on the convention of Fig. 5, V_{dc}^* is 400 kV and the Q_{ref1} is set to 0 MVar. P_{ref2} and Q_{ref2} are set to 400 MW and 0 MVar, respectively. At $t = 0.1$ s, P_{ref2} is ramped from 400 to -400 MW within 0.25 s without changing Q_{ref1} and Q_{ref2} . Then, the system operates in steady-state during $t = 0.35 \sim 0.5$ s. At $t = 0.5$ s, Q_{ref1} is ramped from 0 to -200 MVar within 0.1 s. From $t = 0.6 \sim 0.7$ s system is in steady-state. At $t = 0.7$ s, Q_{ref1} is ramped from -200 to 200 MVar within 0.2 s. The system reaches steady-state after $t = 0.9$ s.

1) *Reactive Power Dependency of DC-Voltage Estimations:* According to Section IV, dc-voltage estimations are affected by reactive power when CCSC is used. The impacts on dc-voltage estimations are demonstrated by applying the described power transients given in Fig. 10(a), under direct dc-

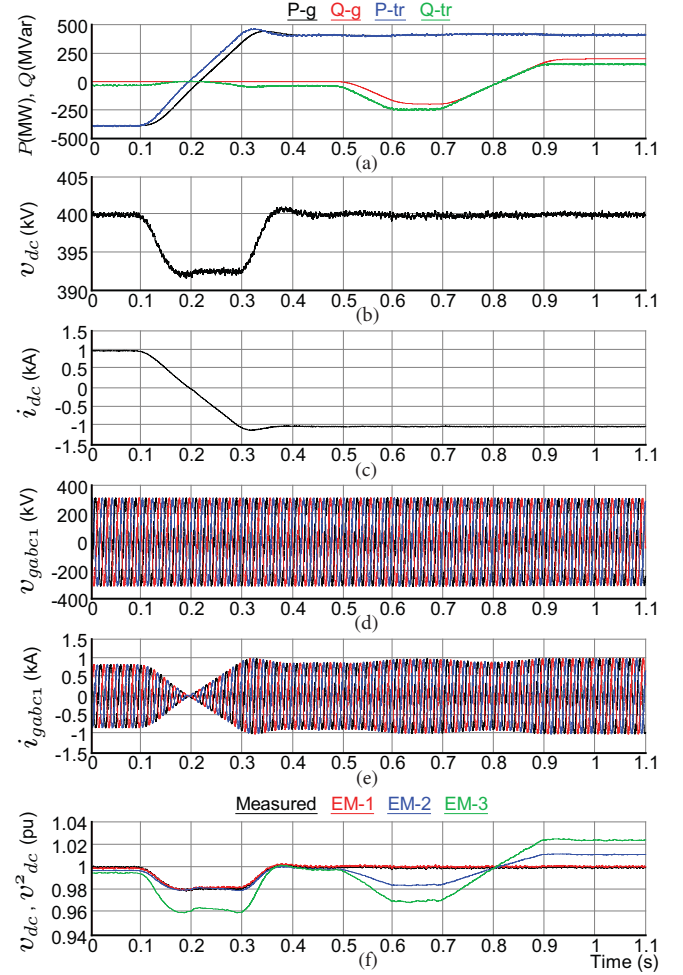


Fig. 10. Active power reversal and reactive power control with direct dc-voltage control and CCSC: (a) active/reactive power at the grid ('-g') and at the converter terminals ('-tr') of MMC-1, (b) dc-voltage, (c) dc current, (d) ac grid voltage, (e) ac grid current and (f) comparison of dc-voltage estimations.

voltage control and CCSC. Fig. 10(f) shows the variations of dc-voltage estimations (EM-1, EM-2, and EM-3) equivalent to changes in P_{ref2} and Q_{ref1} . Only the proposed EM-1 accurately estimates the dc-voltage in all power transients. The estimation errors during the steady-state periods $t = 0.6 \sim 0.7$ s and $t = 0.9 \sim 1.1$ s confirm that EM-2 and EM-3 are significantly influenced by reactive power.

2) *Active/Reactive Power Control with Indirect DC-Voltage Control:* The performance of the estimation methods during the power transients given in Fig. 10 with CCSC and FCCC, are demonstrated in Figs. 11 and 12, respectively.

When CCSC is employed, only EM-1 performs similarly to the direct dc-voltage control for all power transients, as shown in Fig. 11(a). Although EM-2 and EM-3 have steady-state dc-voltage offsets, the transient performances are stable. EM-3 gives the minimum dc-voltage deviation during the power reversal as the indirect regulation parameter is the squared value of dc-voltage. Beyond $t > 0.5$ s, considerably large dc-voltage offsets of EM-2 and EM-3 confirm the impact of reactive power on dc-voltage estimation errors.

Subsequently with FCCC, EM-1 performs similar to the direct dc-voltage control while EM-3 becomes unstable when

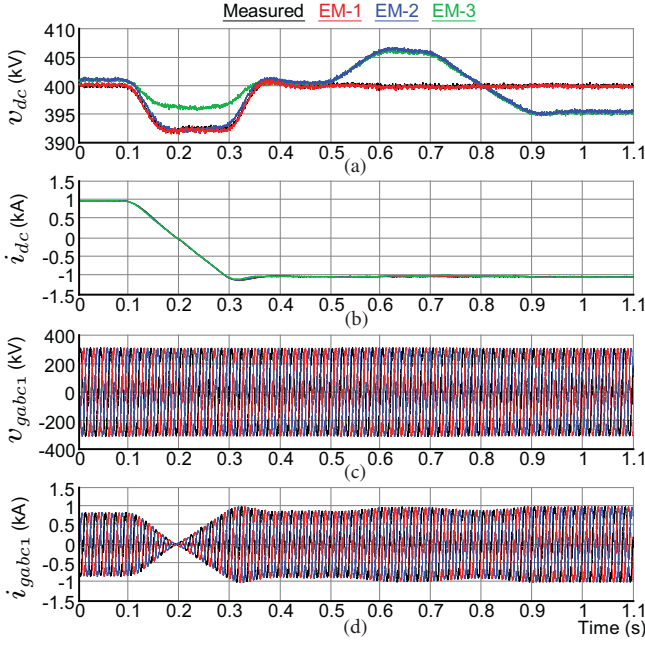


Fig. 11. Dynamic response of indirect dc-voltage control (EM-1,2,3) to active power reversal and reactive power control with CCSC: (a) dc-voltage, (b) dc current, (c) ac grid voltage (EM-1) and (d) ac grid current (EM-1).

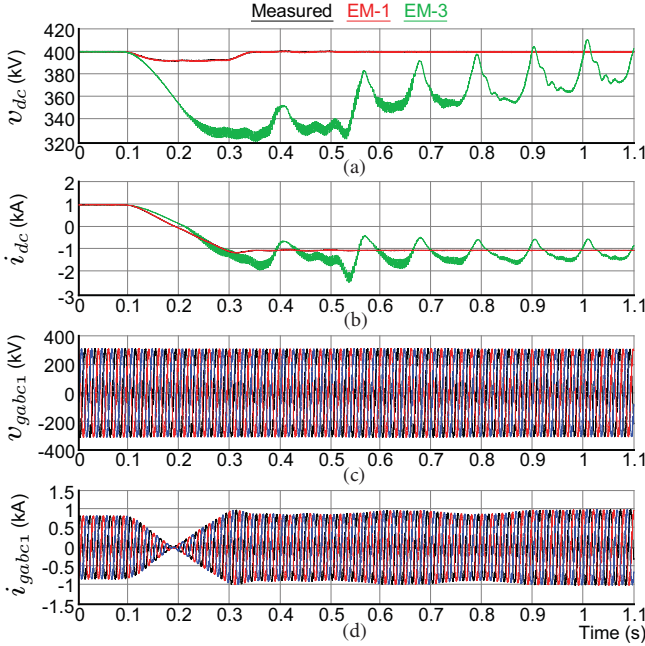


Fig. 12. Dynamic response of indirect dc-voltage control (EM-1,3) to active power reversal and reactive power control with FCCC: (a) dc-voltage, (b) dc current, (c) ac grid voltage (EM-1) and (d) ac grid current (EM-1).

changing P_{ref2} (Figs. 12(a) and (b)) due to the mutual interaction of the dc-voltage controller and the SM capacitor energy regulation loop of FCCC. Moreover, the ac-voltage and current of EM-1 with both CCSC and FCCC, are comparable to those of direct dc-voltage control (Figs. 10(a) and (b)) showing that only EM-1 gives satisfactory performance.

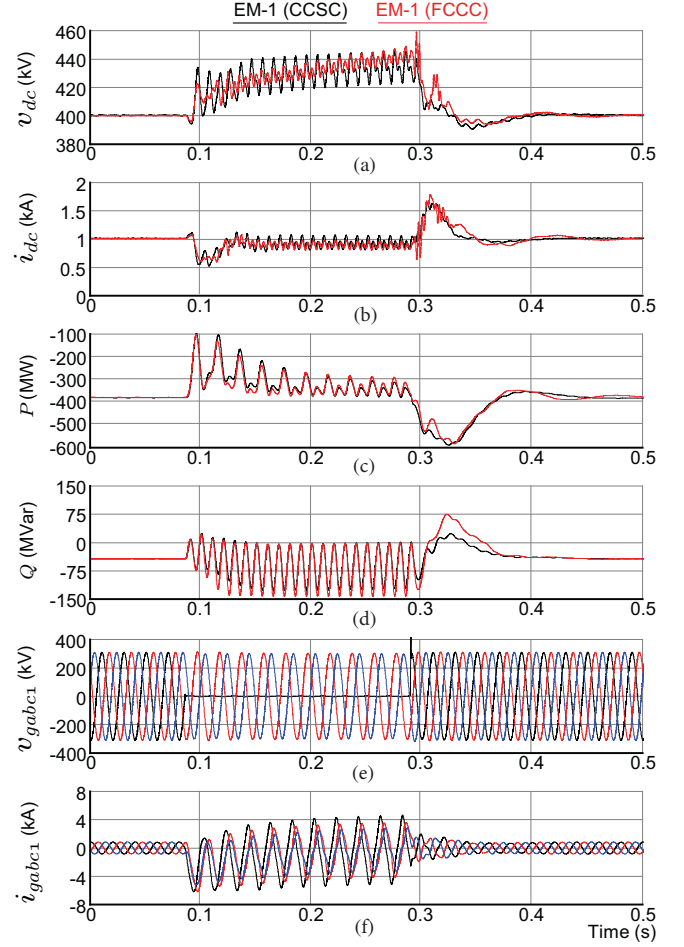


Fig. 13. Dynamic response of EM-1 based indirect dc-voltage control for ac single phase-to-ground fault: (a) dc-voltage, (b) dc current, (c) active power, (d) reactive power, (e) ac grid voltage for EM-1(FCCC) and (f) ac grid current for EM-1(FCCC).

D. Fault Ride-Through Capability

The operation of the MMC-HVDC system under a phase-to-ground fault is considered in this section. At $t = 0.08$ s, a 200 ms phase-to-ground fault occurs at phase-*a* of AC-1, as shown in Fig. 13. During the fault, the dc-voltage ripple with FCCC is small compared to CCSC due to the active SM capacitor voltage regulation of FCCC. The fault responses of EM-2 and EM-3 (not shown) are stable only with CCSC. EM-1 provides fault ride-through (FRT) capabilities regardless of the circulating current controller used.

E. Discussion on Results

Summarizing the presented results, EM-2 and EM-3 both deliver stable performance with CCSC but lead to an estimation error. The major issue is the improper operation of both EM-2 and EM-3 when combined with FCCC as the circulating current controller. The switching function-based EM-1 delivers proper operation under all simulated cases and independent of the circulating current controller. The results for all tests are summarized in Table II, showing the satisfactory performance of EM-1 under both CCSC and FCCC in steady-state, transient

TABLE II
PERFORMANCE COMPARISON OF ESTIMATION METHODS

Operating Conditions	CCSC			FCCC		
	EM-1 (Prop.)	EM-2 (Exis.)	EM-3 (Exis.)	EM-1 (Prop.)	EM-2 (Exis.)	EM-3 (Exis.)
No estimation error	✓	✗	✗	✓	✓	✓
Steady-state performance	✓	✓	✓	✓	✗	✓
P and Q transients	✓	✓	✓	✓	✗	✗
AC-fault ride-through	✓	✓	✓	✓	✗	✗

TABLE III
CALCULATED AND SIMULATED ESTIMATION ERROR

Estimation Error (%)		CCSC		FCCC	
		p.f=1	p.f=0.85	p.f=1	p.f=0.85
$v_{dc(EM-1)}$ (Proposed)	Calculated	0	0	0	0
	Simulated	0.04	0.03	0.04	0.03
$v_{dc(EM-2)}$ (Existing)	Calculated	0.22	1.60	0	0
	Simulated	0.24	1.67	0.03	0.05
$v_{dc(EM-3)}^2$ (Existing)	Calculated	0.44	3.19	0	0
	Simulated	0.49	3.20	0.01	0.01

and fault conditions. The above results can be summarized as follows.

- EM-1 delivers good performance for all simulated operating conditions regardless of the type of circulating current controller.
- EM-2 and EM-3 have satisfactory performance under steady-state, power transients, and FRT only with CCSC but introduce a reactive power dependent estimation error as explained in Section IV-B.
- EM-2 and EM-3 do not deliver satisfactory performance when combined with FCCC due to the interaction between dc-voltage estimation and circulating current control.
- FCCC is capable of reducing the estimation error of all dc-voltage estimation methods due to its active SM capacitor voltage regulation capability which compensates for the overall dc offset of the SM capacitor voltages as shown in (22) and Section IV-C.

A summary of the calculated and simulated results for the MMC-HVDC system based on Section IV-B and Fig. 7 is presented in Table III. The impact of reactive power on the estimation error becomes more apparent, with increased estimation errors for non-unity power factor operation under CCSC. The active SM capacitor voltage regulation capability of FCCC compensates for the reactive power dependent estimation error leading to almost zero estimation error.

VI. CONCLUSION

Estimation-based indirect dc-voltage control in MMCs interacts with circulating current control methods due to the close relation between SM capacitor voltages and the power fluctuations in MMC arms. This paper proposes an estimation method for the dc-link voltage of the MMC combined with indirect dc-voltage control. The comparison with alternative approaches demonstrates that; i) The proposed method offers similar performance as direct dc-voltage measurement avoiding mutual interactions regardless of the circulating current controller, due to the use of SM switching function in estimating the dc-voltage. ii) The alternative dc-voltage estimation methods suffer from a reactive power dependent estimation error, and the error cannot be compensated by CCSC due to the lack of SM capacitor voltage regulation capability. iii) FCCC is able to compensate for the overall estimation error as the dc component of the SM capacitor voltages is actively regulated.

REFERENCES

- [1] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.
- [2] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Power Tech Conf.*, vol. 3, Jun. 2003.
- [3] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.
- [4] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015.
- [5] G. P. Adam and I. E. Davidson, "Robust and generic control of full-bridge modular multilevel converter high-voltage dc transmission systems," *IEEE Trans. Power Del.*, vol. 30, no. 6, pp. 2468–2476, Dec. 2015.
- [6] G. Konstantinou, J. Zhang, S. Ceballos, J. Pou, and V. G. Agelidis, "Comparison and evaluation of sub-module configurations in modular multilevel converters," in *Proc. IEEE-PEDS Conf.*, Jun. 2015, pp. 958–963.
- [7] S. Cui and S. K. Sul, "A comprehensive dc short-circuit fault ride through strategy of hybrid modular multilevel converters (MMCs) for overhead line transmission," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7780–7796, Nov. 2016.
- [8] Z. Yuebin, J. Daozhuo, G. Jie, H. Pengfei, and L. Zhiyong, "Control of modular multilevel converter based on stationary frame under unbalanced ac system," in *Proc. IEEE-ICDMA Conf.*, Jul. 2012, pp. 293–296.
- [9] S. Li, X. Wang, Z. Yao, T. Li, and Z. Peng, "Circulating current suppressing strategy for MMC-HVDC based on nonideal proportional resonant controllers under unbalanced grid conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 387–397, Jan. 2015.
- [10] J. W. Moon, J. W. Park, D. W. Kang, and J. M. Kim, "A control method of HVDC-modular multilevel converter based on arm current under the unbalanced voltage condition," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 529–536, Apr. 2015.
- [11] A. Antonopoulos, L. Angquist, and H. P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Proc. IEEE-EPE Conf.*, Sep. 2009, pp. 1–10.
- [12] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 777–788, Feb. 2015.
- [13] S. Cui, S. Kim, J. J. Jung, and S. K. Sul, "A comprehensive cell capacitor energy control strategy of a modular multilevel converter (MMC) without a stiff DC bus voltage source," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Mar. 2014, pp. 602–609.

- [14] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.
- [15] B. Bahrani, S. Debnath, and M. Saeedifard, "Circulating current suppression of the modular multilevel converter in a double-frequency rotating reference frame," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 783–792, Jan. 2016.
- [16] G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Arzande, J. C. Vannier, and M. Molinas, "An energy-based controller for HVDC modular multilevel converter in decoupled double synchronous reference frame for voltage oscillation reduction," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2360–2371, Jun. 2013.
- [17] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, R. Picas, and V. G. Agelidis, "A modified voltage balancing algorithm for the modular multilevel converter: Evaluation for staircase and phase-disposition PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4119–4127, Aug. 2015.
- [18] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.
- [19] F. Deng and Z. Chen, "A control method for voltage balancing in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 66–76, Jan. 2014.
- [20] S. Cui, J.-J. Jung, Y. Lee, and S.-K. Sul, "A novel control strategy of a modular multilevel converter (MMC) based VSC-HVDC transmission system," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2015, pp. 972–979.
- [21] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.
- [22] K. Sekiguchi, P. Khamphakdi, M. Hagiwara, and H. Akagi, "A grid-level high-power BTB (back-to-back) system using modular multilevel cascade converters without common dc-link capacitor," *IEEE Trans. Ind. Electron.*, vol. 50, no. 4, pp. 2648–2659, Jul. 2014.
- [23] G. Bergna, M. Boyra, and J. H. Vivas, "Evaluation and proposal of MMC-HVDC control strategies under transient and steady state conditions," in *Proc. IEEE-EPE Conf.*, Aug. 2011, pp. 1–10.
- [24] S. Samimi, F. Gruson, P. Delarue, F. Colas, M. M. Belhaouane, and X. Guillaud, "MMC stored energy participation to the DC bus voltage control in an HVDC link," *IEEE Trans. Power Del.*, vol. 31, no. 4, pp. 1710–1718, Aug. 2016.
- [25] G. Konstantinou, J. Pou, S. Ceballos, R. Darus, and V. G. Agelidis, "Switching frequency analysis of staircase-modulated modular multilevel converters and equivalent PWM techniques," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 28–36, Feb. 2016.
- [26] B. Chuco and E. H. Watanabe, "Back-to-back HVDC based on modular multilevel converter," in *Proc. IEEE-COBEF Conf.*, Sep. 2011, pp. 970–976.
- [27] L. Michels, R. F. de Camargo, F. Botteron, H. A. Grudling, and H. Pinheiro, "Generalised design methodology of second-order filters for voltage-source inverters with space-vector modulation," *IEE Proc. Electr. Power Appl.*, vol. 153, no. 2, pp. 219–226, Mar. 2006.
- [28] R. Li and J. E. Fletcher, "A novel MMC control scheme to increase the DC voltage in HVDC transmission systems," *Electric Power Systems Research*, vol. 143, pp. 544–553, Feb. 2017.
- [29] G. Konstantinou, H. R. Wickramasinghe, S. Ceballos, and J. Pou, "Offset PWM in modular multilevel converters for stored arm energy reduction," in *Proc. 2016 IEEE 2nd Annual Southern Power Electronics Conf. (SPEC)*, Dec. 2016, pp. 1–6.
- [30] CIGRE Working Group B4.57, "Guide for the development of models for HVDC converters in a HVDC grid," 2014.



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